

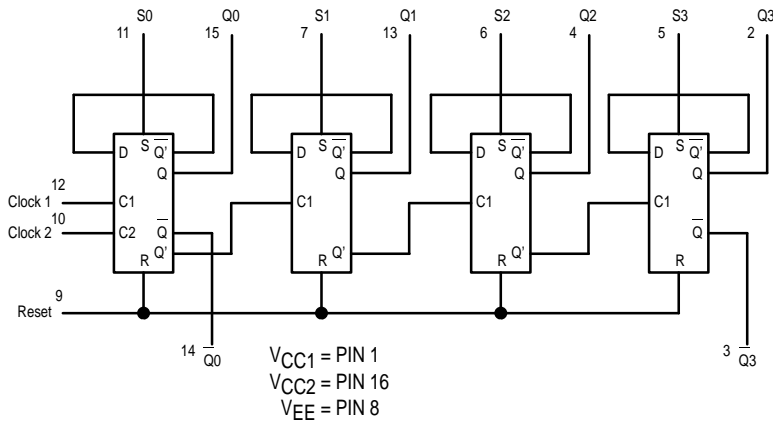
Binary Counter

The MC10154 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

$P_D = 370 \text{ mW typ/pkg (No Load)}$
 $f_{\text{toggle}} = 150 \text{ MHz (typ)}$
 $t_{pd} = 3.5 \text{ ns typ (C to } Q_0)$
 $t_{pd} = 11 \text{ ns typ (C to } Q_3)$

LOGIC DIAGRAM

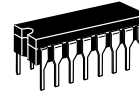


TRUTH TABLE

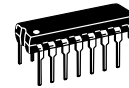
INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	X	X	L	L	L	L
L	H	H	H	H	X	X	H	H	H	H
L	L	L	L	L	H	X	No Count			
L	L	L	L	L	X	H	No Count			
L	L	L	L	L	*	*	H	H	H	H
L	L	L	L	L	*	*	L	H	H	H
L	L	L	L	L	*	*	H	L	H	H
L	L	L	L	L	*	*	L	L	H	H
L	L	L	L	L	*	*	H	H	L	H
L	L	L	L	L	*	*	L	H	L	H
L	L	L	L	L	*	*	H	L	L	H
L	L	L	L	L	*	*	L	L	L	H
L	L	L	L	L	*	*	H	H	H	L
L	L	L	L	L	*	*	L	H	H	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	H	L	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	L	L	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	L	L	L

* Clock transitions from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

MC10154

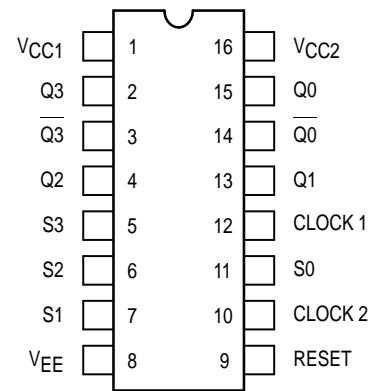


L SUFFIX
CERAMIC PACKAGE
CASE 620-10



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		97			88		97	mAdc
Input Current	I _{inH}	12		390			245		245	μAdc
		11		350			220		220	
		9		650			410		410	
	I _{inL}	*	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V _{OH}	14	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		15	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	V _{OL}	14	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	V _{OHA}	3	-1.080		-0.980			-0.910		Vdc
		14	-1.080		-0.980			-0.910		
		15	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	V _{OLA}	3		-1.655			-1.630		-1.595	Vdc
		14		-1.655			-1.630		-1.595	
		15		-1.655			-1.630		-1.595	
Switching Times (50Ω Load)										ns
Clock Input Propagation Delay	t ₁₂₊₁₅₊ t ₁₂₋₁₃₋ t ₁₂₊₄₋ t ₁₂₋₃₊	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	
		13	1.9	9.4	2.0	6.0	9.2	2.0	9.8	
		4	2.9	12.3	3.0	8.5	12.0	3.0	12.8	
		3	3.9	14.9	4.0	11.0	14.5	4.0	15.5	
Rise Time (20 to 80%)	t ₁₅₊	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)	t ₁₅₋	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Set Input	t ₁₁₋₁₅₊	15	1.4	5.2	1.5		5.0	1.5	5.5	
Reset Input	t ₉₋₁₅₊	15	1.4	5.2	1.5		5.0	1.5	5.5	
Counting Frequency	f _{count}	15	125		125	150		125		MHz

* Individually test each input applying V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

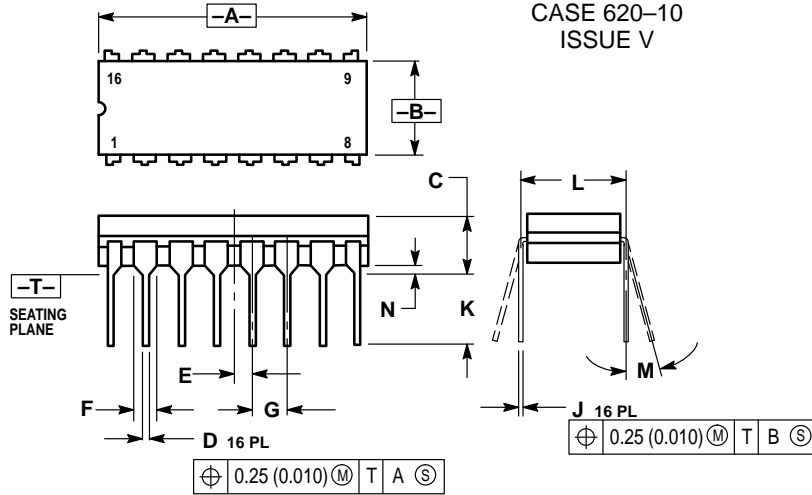
			TEST VOLTAGE VALUES (Volts)					V_{CC} Gnd			
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{EE}				
@ Test Temperature											
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2				
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2				
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2				
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW								
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{EE}				
Power Supply Drain Current	I_E	8	9				8	1, 16			
Input Current	I_{inH}	12	12				8	1, 16			
		11	11				8	1, 16			
9		9				8	1, 16				
	I_{inL}	*		*			8	1, 16			
Output Voltage	Logic 1	V_{OH}	14	9				8	1, 16		
			15	11				8	1, 16		
Output Voltage	Logic 0	V_{OL}	14	11				8	1, 16		
			15	9				8	1, 16		
Threshold Voltage	Logic 1	V_{OHA}	3			5		8	1, 16		
			14			11		8	1, 16		
			15			9		8	1, 16		
Threshold Voltage	Logic 0	V_{OLA}	3				5	8	1, 16		
			14				11	8	1, 16		
			15				9	8	1, 16		
Switching Times (50Ω Load)											
Clock Input Propagation Delay						Pulse In	Pulse Out	-3.2 V	+2.0V		
						t_{12+15+}	15	12	15	8	1, 16
						t_{12-13-}	13	12	13	8	1, 16
						t_{12+4-}	4	12	4	8	1, 16
						t_{12-3+}	3	12	3	8	1, 16
Rise Time (20 to 80%)											
t_{15+}	15	12	15	8	1, 16						
Fall Time (20 to 80%)											
t_{15-}	15	12	15	8	1, 16						
Set Input											
t_{11-15+}	15	11	15	8	1, 16						
Reset Input											
t_{9-15+}	15	9	15	8	1, 16						
Counting Frequency											
f_{count}	15	12	15	8	1, 16						

* Individually test each input applying V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

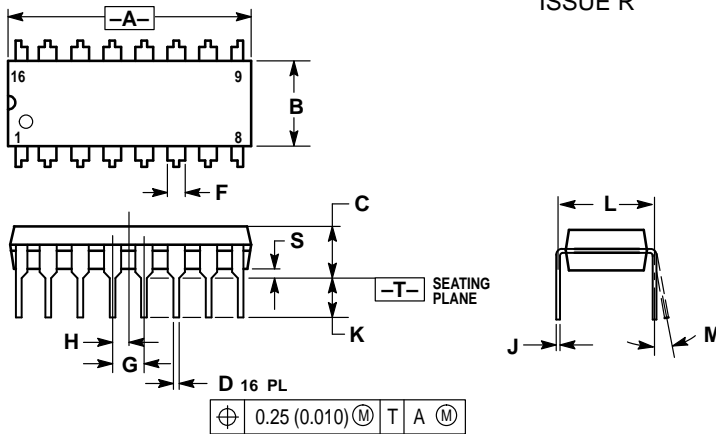
L SUFFIX
CERAMIC DIP PACKAGE
 CASE 620-10
 ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
 CASE 648-08
 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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